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Built-in Self-Test (Part 1)

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~~1 5 ReferenceDedication~~

~~(*optional) Floor planning~~

~~12 1 DFT2 JTAG Intro~~

STICK DIAGRAM - simplified
(VLSI)

11 3 DFT1 - Test Mode

Operation (SSF \u0026 Delay

Test LOS/LOC) Design Rule

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Check VLSI – Lecture 4:

Design Metrics ~~1-2~~

~~Introduction Types Of Tests~~

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Design for Testability Test

Pattern Generation The Scope

\u0026 Career Opportunities

For Physical Design in VLSI

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14 4 BIST2 Architecture

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Bushnell Lecture 12: DFT and Scan 4 Scan Design Scan Design Circuit is designed using pre-specified design rules. Test structure (hardware) is added to the verified design: Add a test control (TC) primary input.

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Replace flip-flops by scan flip-flops (SFF) and connect to form one or more shift registers in the test mode. Make input/output of each scan shift register controllable/observable from PI/PO. Use combinational

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