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parallel load input = 1, the

clock pulses go through the

AND gate and the data inputs

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are loaded into the register when the parallel load input = 0, the output of the AND gate remains at 0. 2.10. The buffer gate does not perform logic. It is

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11. Change the AND gates to

NAND gates. The rest of the

circuit is unchanged. 12.

Remove the tri-state buffers

and do one of the following:

a) Change each 2-input AND

gate to a 3-input AND gate.

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