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[Dc Shell User Guide - happybabies.co.za](http://happybabies.co.za)

[Dc Shell User Guide - agnoleggio.it](http://agnoleggio.it) For more information on the compile ultra command consult the Design Compiler User Guide (`dc-user-guide.pdf`) or use `man compile ultra` at the DC shell prompt. Run the following command and take a look at the output. DC will attempt to synthesize your design while `dc_shell.html - Ip`

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Design Compiler User Guide dc\_shell> write -hierarchy -output

my\_design.db To exit dc\_shell, do one of the following: • Enter

quit. • Enter exit. • Press Ctrl-d. When you exit dc\_shell, text

similar to the following appears (the memory and the CPU numbers

re?ect your actual usage): Memory

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The following command tells # the tool that the pin named clk is the

clock and that the desired clock # period is 1 nanosecond. dc\_shell-

topo> create\_clock clk -name ideal\_clock1 -period 1 # The

compile\_ultra command begins the actual synthesis process that #

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transforms your design into a gate-level netlist.

## RTL-to-Gates Synthesis using Synopsys Design Compiler

4 User Commands dc\_shell-t Invokes the Design Compiler shell in dctcl mode. For more information, see the man page for dc\_shell.

```
dc_shell-t [-f script_file] [-x command_string] [-no_init] [-checkout  
feature_list] [-wait wait_time] [-timeout timeout_value] [-version]  
[-behavioral] [-fpga] [-syntax_check | -context_check] dc_shell
```

## Synthesis Quick Reference - Computer Science

dc\_shell -f scriptFile Most efficient and common usage is to put  
TCL commands into scriptFile ,including “quit” at the end TCL =  
Tool Command Language Edit and rerun scriptFile as needed GUI  
version (Design Vision) design\_vision From dc\_shell: gui\_start



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Main advantage over dc\_shell is to view the synthesized schematic

## Automated Synthesis from HDL models

CS250 Tutorial 5 (Version 091210b) September 12, 2010 Yunsup Lee. In this tutorial you will gain experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate-level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design.

## RTL-to-Gates Synthesis using Synopsys Design Compiler

For more information on the compile command consult the Design Compiler User Guide (dc-user-guide.pdf) or use man compileat the

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DC shell prompt. Run the following command and take a look at the output. `dc_shell-xg-t> compile -map_effort medium -area_effort medium` The compile command will report how the design is being optimized.

### RTL-to-Gates Synthesis using Synopsys Design Compiler

the compileultra command consult the Design Compiler User Guide (dc-user-guide.pdf) or use `man compileultra` at the DC shell prompt. Run the following command and take a look at the output. DC will attempt to synthesize your design while still meeting the constraints. DC considers two

### RTL-to-Gates Synthesis using Synopsys Design Compiler

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Guide dc\_shell. The dc\_shell supports two scripting languages – dcsh, which uses the Synopsys language, and dctcl, which uses Tcl (Tool Command Language). It is recommended that Design Analyzer be used for most of the synthesis and optimization processes. The dc\_shell is preferable for a standardized synthesis

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```
%> dc shell -t any memory LIB file %> dc_shell dc_shell-t>
read_lib t13spsram512x32_slow_syn.lib dc_shell-t> write_lib
t13spsram512x32 -output \ t13spsram512x32_slow_syn.db Modify
<.synopsys_dc.setup> File: “* user library name, which should be
the same as the library name in the Artisan set link_library slow.db
```

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t13spsram512x32\_slow.db

Training Course of Design Compiler [????]

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Dc Shell User Guide - powsgurh.qibumr.channelbrewing.co

View Dc\_shell commands from ELECTRONICS 121 at Rajasthan Technical University. # #Design Compiler settings can be in .synopsys\_dc.setup # #Reading design file read\_verilog

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golden\_arbiter.v #Pointing

Dc shell commands - #Design Compiler settings can be in ...

Figure 1.1 Workflow of DC We use Synopsys Design Compiler (DC) to synthesize Verilog RTL models into a gate-level netlist where all of the gates are from the standard cell library. So

Synopsys DC ... % dc\_shell-t -f <file>.tcl In the above example, it should be: % dc\_shell-t -f compiledc.tcl

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...

In the preceding example, a dedicated wrapper cell is used. Chapter 8: Wrapping Cores Core Wrapping Flows 8-13 DFT Compiler Scan User Guide Version H-2013.03-SP4 To prevent the insertion of

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wrapper cells for a specific list of ports, use the following command: `dc_shell> set_boundary_cell -class core_wrapper \ -ports port_list -type none` This might be needed in cases where an output port drives downstream clock pins or asynchronous set or reset signals.

[dcshell set linklibrary mytechlibdb dwfoundationsldb ...](#)

Design Compiler Graphical extends DC Ultra™ topographical technology to produce physical guidance to the IC Compiler place-and-route solution, tightening timing and area correlation to 5% while speeding-up IC Compiler placement by 1.5X.

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