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Q. 5.10: A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z  
Q. 5.6: A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is  
Q. 5.1: The D latch of Fig. 5.6 is constructed with four NAND

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~~gates and an inverter.~~

~~Consider the Q. 4.8: Design a  
code converter that converts  
a decimal digit from the 8,  
4, -2, -1 code to BCD Q.~~

5.4: A PN flip-flop has four  
operations: clear to 0, no  
change, complement, and set  
to 1, when Q. 5.8: Derive  
the state table and the  
state diagram of the  
sequential circuit shown in  
Fig. P5.8

---

Q. 4.26: Construct a  
4-to-16-line decoder with  
five 2-to-4-line decoders  
with enable.

---

Digital Logic Design - Unit  
04 - Combinational Logic -  
Part 05 - Binary Multiplier,  
Magnitude CompaBook M Morris  
Mano index Q. 3.9: Find all

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*the prime implicants for the following Boolean functions, and determine which are Q.*

*4.34: Implement the following Boolean function with a multiplexer (HDL—see Problem 4.48) What Is*

*Digital Design? - Depend*

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*diagram/state table/circuit*

*diagram (using D-flip flop)*

*- Digital Logic Design*

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Implementation of 5x32  
decoder using 3x8 and 2x4  
decoder ~~Combinational  
circuit with decoder and  
external logic gates~~  
~~Digital Electronics Example~~  
*Q. 3.11: Simplify the  
following Boolean functions:  
using five variable maps:*  
(a)  $F(A,B,C,D,E) = \text{Sum}$   
*Solutions Manual Digital  
Design With an Introduction  
to the Verilog HDL 5th  
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*Q. 1.1: List the octal and  
hexadecimal numbers from 16*

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~~to 32. Using A and B for the last two digits Q. 7.19:~~

~~Tabulate the PLA programming table for the four Boolean functions listed below. Q.~~

~~3.15: Simplify the following Boolean function F, together with the don't care conditions d, and~~

---

Digital Design: Q. 1.13: Do the following conversion problems: (a) Convert

decimal 27.315 to binary

~~Design of Digital Circuits—~~

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