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In the receiver side, detection of flag bits marks the beginning of new frame and zero unstuffing of data is performed. The unstuffed data is stored in variable length memory. The architecture for HDLC protocol has been proposed in this paper. The proposed model is implemented and verified using Verilog HDL.

Implementation of HDLC controller design using Verilog HDL ...  
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Verilog HDL based FPGA design - IEEE Conference Publication  
ABSTRACT This paper presents a design of Dual tree Complex wavelet transform (DTCWT) implemented in VLSI architecture using Verilog HDL and result in verified in FPGA implementation which achieves approximate shift invariance and good directionality.

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In this paper, the design and the implementation of various 32-bit adders like Ripple Carry Adder (RCA), Carry Increment adder (CINA) and Carry bypass adder (CBYA) for different full adder cells is done using the Verilog HDL. The results are obtained by executing Verilog code in Xilinx 14.5 ISE for the Spartan 3E family device with speed grade -5.

Design and implementation of 32-bit adders using various ...  
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This paper describes the design and validation of a complex ASIC through the use of Verilog HDL. The CMC is an interface circuit for ATM cells, part of a 2.5 Gb/s switching fabric. Its main function is serial to parallel and parallel to serial data conversion; another features like VPINCI translation, cell counting, insertion and extraction from an external microprocessor are also included.

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Implementation and Performance Analysis of RSA Algorithm Using Verilog free download ABSTRACT This paper proposes an efficient method to implement RSA decryption algorithm. RSA cryptosystem is the most attractive and popular security technique for many applications, such as electronic commerce and secure internet access. There are few end- Design of a Modified Gabor Filter with Vedic Multipliers Using Verilog HDL

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